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REMARKS

Entry of this Amendment if proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 11-18 and 26-31 and 33-38 are all the claims presently pending in the application. Claims 29 and 35 have been amended to more particularly define the invention. Claim 32 has been canceled.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 11-12, 15-16, 18, 26, 28-29, 32-33 and 36-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al. (U.S. Patent No. 5,940,319). Claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Bronner, et al. (U.S. Patent No. 6,242,770). Claims 34-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Oda (U.S. Patent No. 5,994,749).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (as recited in claim 11) is directed to an array of microelectronic elements which includes a substrate of semiconductor material, a lower layer of dielectric material disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto, a pattern of mutually electrically isolated conductive regions disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer, and a plurality of nodes of semiconductor material disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer.

Each conducting region includes a metal conductor, and a via including a diffusion

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barrier material. Importantly, the diffusion barrier material extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node.

Conventional devices do not include a diffusion barrier between a metal conductor (e.g., a word line) and a semiconductor node (e.g., a silicon diode). Thus, the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.

To address this problem, the metal conductor (e.g., word line) may be made from a refractory metal. However, such refractory metal word lines have a high resistance, such that only small arrays of memory elements can be made (Application at page 8, lines 10-13).

The claimed invention, on the other hand, includes a via formed on the metal conductor and including a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. The diffusion barrier material keeps the conductive region from reacting with the semiconductor material in the node. Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum, for improved performance.

II. THE PRIOR ART REFERENCES

A. The Durlam Reference

The Examiner alleges that Durlam teaches the claimed invention as recited in claims 11-12, 15-16, 18, 26, 28-29, 33 and 36-38. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Durlam.

Durlam discloses a magnetic random access memory (MRAM) which includes magnetic memory elements. A digit line and bit line are placed under and on top of the memory element. The lines are enclosed by a high permeability layer excluding a surface facing the memory element, which shields and focuses a magnetic field toward the memory element (Durlam at Abstract).

However, contrary to the Examiner's allegations, Durlam does not teach or suggest a conductive via which includes a "*diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node*" as recited, for example, in claim 11 and similarly recited in claim 26.

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As noted above, conventional devices do not include a diffusion barrier between a metal conductor (e.g., a word line) and a semiconductor node (e.g., a silicon diode). Thus, the metal conductor reacts with the semiconductor node making the devices unreliable. As a result, the metal conductor is commonly made from a refractory metal which has a high resistance. (Application at page 3, lines 3-9; page 8, lines 7-8).

The claimed invention, on the other hand, includes a via formed on the metal conductor and including a diffusion barrier material which extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node. (Application at page 8, lines 3-16; Figure 5B). This via may be formed, for example, of refractory metal. Further, as illustrated in the exemplary embodiment of Figure 5A-5B, the via may be filled with the diffusion barrier material (Application at page 8, lines 3-15).

The diffusion barrier material keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum for improved performance (Application at page 8, lines 3-16).

Clearly, Durlam does not teach or suggest these novel features. Indeed, Durlam does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

The Examiner attempts to rely on Figures 5-8 in Durlam to support his allegations. Specifically, the Examiner attempts to equate the metal conductor 37 in Durlam with the via in the conducting region of the claimed invention (e.g., via 13 in the exemplary embodiment illustrated in Figures 5A-5B of the Application). However, the Examiner is completely incorrect.

In particular, the Examiner relies on col. 3, lines 35-42 to support his allegation that the via includes Ta (e.g., a diffusion barrier material). However, this passage merely refers to Figure 3, stating:

“In order to improve adhesion of field focusing layer 24 and to provide a barrier for Ni or Fe diffusion into the conductor and/or dielectric a layer of

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Ta or TaN or such materials could be added between field focusing layer 24 and conductor layer 26" (Durlam at col. 3, lines 39-42).

Applicant notes that conductor layer 26 eventually becomes the metal conductor 37 illustrated in Figure 5 in Durlam. Therefore, Durlam merely teaches that a "barrier" may be provided before forming the metal conductor 37. That is, nowhere does this passage or Figure 3 in Durlam teach or suggest that the metal conductor 37 includes barrier material.

Moreover, even if it is assumed (arguendo) that the metal conductor 37 includes a diffusion barrier material, the metal conductor 37 still cannot reasonably be equated with the via of the claimed invention. Indeed, as recited in claim 11, in the claimed invention, the via extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node. (Application at page 8, lines 3-16; Figure 5B). In fact, the via in the claimed invention may be used to prevent the metal conductor from reacting with a semiconductor node, such as a silicon diode.

Durlam, on the other hand, teaches that the metal conductor 37 is used to "electrically connect plug conductors 19a and 19b to conductor layer 34" (Durlam at col. 3, line 67). That is, the metal conductor 37 electrically connects the plug conductors 19a, 19b to the metal conductor layer 45, as illustrated in Figure 7 (e.g., see Durlam at Abstract). Therefore, the function of the metal conductor 37 is completely different than the function of the via in the claimed invention.

For example, in the exemplary embodiment illustrated in Figure 5A, the via includes a diffusion barrier material which extends between the word line 15 and a diode mesa including Si layer 3'. Thus, the via may be used to electrically connect the metal conductor with the semiconductor node.

In fact, the Examiner expressly concedes that the portion of Durlam on which he is relying as disclosing the claimed invention, does not teach or suggest this feature. However, the Examiner surprisingly refers to a completely unrelated aspect of Durlam as allegedly disclosing this feature. Specifically, the Examiner alleges that this feature is disclosed in Figure 17 of Durlam which is completely unrelated to the embodiment in Figure 5 of Durlam.

Applicant respectfully reminds the Examiner that he can not merely search throughout a reference willy-nilly, and picking and choosing unrelated features to somehow kluge

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together a basis for his rejection. Here, the Examiner is relying on alleged features from completely unrelated and different aspects to support his position, which cannot form the basis for his rejection. Clearly, the embodiment of Figure 17 would not have been combined with the unrelated embodiment of Figure 5, and the Examiner has failed to provide any adequate motivation or suggestion for such combination.

Moreover, even assuming that the embodiment of Figure 17 would have been combined with the embodiment of Figure 5, the alleged combination would not teach or suggest a conductive via which includes "*diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node*".

Indeed, Figure 17 does not even teach or suggest a "via" as in the claimed invention, but instead illustrates a diode 95 formed directly on a metal conductor 82. Certainly, Figure 17 does not teach or suggest a via which includes a diffusion barrier material extending between a metal conductor and a semiconductor node.

Therefore, contrary to the Examiner's allegations, nowhere does Durlam teach or suggest the conductive via of the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Durlam. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Bronner Reference

The Examiner alleges that Durlam would have been combined with Bronner to form the claimed invention as recited in claims 13-14, 17, 27 and 30-31. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Bronner discloses a magneto-resistive memory cell which includes a substrate, monocrystalline diode formed in the substrate, a first conductor in the substrate and a second conductor formed above a magnetic tunnel junction formed on the diode (Bronner at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters.

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Specifically, the Durlam device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), whereas Bronner is intended to minimize the resistance of a diode in a memory cell (Bronner at col. 3, lines 3-4). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that “[i]t would have been obvious to form Durlam’s diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes ... would provide high conductivity, high rectification, and low total resistance” which is insufficient to support the combination.

Moreover, neither Durlam, nor Bronner, nor any combination thereof teaches or suggests a conductive via which includes a “*diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node*” as recited, for example, in claim 11 and similarly recited in claim 26.

As noted above, unlike conventional devices which do not include a diffusion barrier between a metal conductor (e.g., a word line) and a semiconductor node (e.g., a silicon diode), the claimed invention, includes a via formed on the metal conductor and including a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. (Application at page 8, lines 3-16; Figure 5B). Further, as illustrated in the exemplary embodiment of Figure 5A-5B, the via may be filled with the diffusion barrier material (Application at page 8, lines 3-15).

The diffusion barrier material keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum for improved performance (Application at page 8, lines 3-16).

Clearly, Bronner does not teach or suggest these novel features. Indeed, Bronner does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to

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address.

Further, Applicant notes that the Examiner merely relies on Bronner as allegedly disclosing a single crystal Si diode. That is, the Examiner is not relying on Bronner as disclosing the novel features of the claimed invention.

In addition, Bronner merely discloses a diode 514 which is in the shape of a V-groove formed in an insulation layer 100. A metal conductor 525 is formed on the diode 514 and an oxide layer 530 is formed on the metal conductor 525 (Bronner at Figure 5B). This structure is completely unrelated to the claimed invention.

Therefore, Bronner clearly does not teach or suggest a via formed on the metal conductor and including a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. Thus, Bronner clearly does not make up for the deficiencies of Durlam.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Oda Reference

The Examiner alleges that Oda would have been combined with Durlam to form the claimed invention as recited in claims 34-35. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Oda discloses a semiconductor device which includes a semiconductor substrate having an element region and source and drain regions, a gate dielectric film containing nitrogen formed in the element region of said semiconductor substrate, a gate electrode formed on the gate dielectric film, and three dielectric films (Oda at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters.

Specifically, the Durlam device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), whereas Oda is merely intended to prevent nitrogen from diffusing out of a gate oxide and gate electrode

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(Oda at col. 3, lines 5-23). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that “[i]t would have been obvious to form Durlam’s diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes ... would provide high conductivity, high rectification, and low total resistance” which is insufficient to support the combination.

Moreover, neither Oda, nor Bronner, nor any combination thereof teaches or suggests a conductive via which includes a “*diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node*” as recited, for example, in claim 11 and similarly recited in claim 26.

As noted above, unlike conventional devices, the claimed invention includes a via formed on the metal conductor a including a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. (Application nd at page 8, lines 3-16; Figure 5B). Further, as illustrated in the exemplary embodiment of Figure 5A-5B, the via may be filled with the diffusion barrier material (Application at page 8, lines 3-15).

Clearly, Oda does not teach or suggest these novel features. Indeed, Oda does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

Further, Applicant notes that the Examiner merely relies on Oda as allegedly disclosing a metal conductor which is formed of a different material than the via. That is, the Examiner is not relying on Oda as disclosing the novel features of the claimed invention.

In addition, Oda merely discloses device having a gate electrode film containing nitrogen. Nowhere does Oda teach or suggest microelectronic element array, let alone a via formed on a metal conductor (e.g., word line) and including a diffusion barrier material which extends between the metal conductor and a node and electrically connects the metal conductor with the node. Thus, Oda clearly does not make up for the deficiencies of Durlam.

Therefore, Applicant submits that these references would not have been combined and

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even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 11-18 and 26-31 and 33-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 4/27/04



Phillip E. Miller
Registration No. 46,060

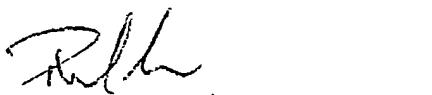
McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Phat X Cao , Group Art Unit # 2814 at fax number (703) 872-9306 this 27th day of April, 2005.



Phillip E. Miller
Reg. No. 46,060